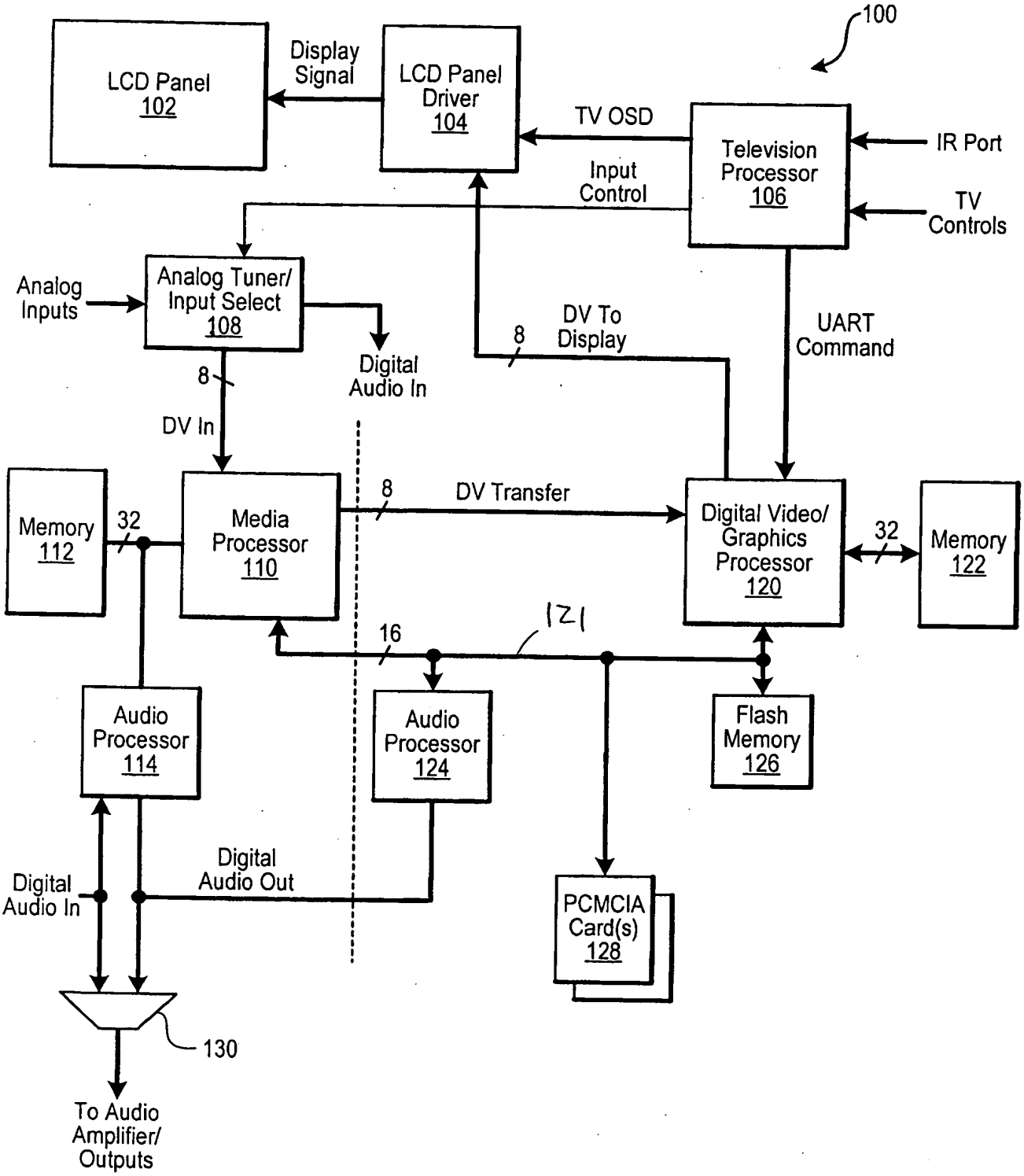
100
LCD Panel
102
Display
Signal
LCD Panel
Driver
104
TV OSD
Television
Processor
106
IR Port
Input
Control
TV
Controls
Analog
Inputs
Analog Tuner/
Input Select
108
Digital
Audio In
8
DV In
DV To
Display
8
UART
Command
Memory
112
32
Media
Processor
110
8
DV Transfer
Digital Video/
Graphics
Processor
120
32
Memory
122
16
121
Audio
Processor
114
Audio
Processor
124
Flash
Memory
126
Digital
Audio In
Digital
Audio Out
PCMCIA
Card(s)
128
130
To Audio
Amplifier/
Outputs

Fig. 1

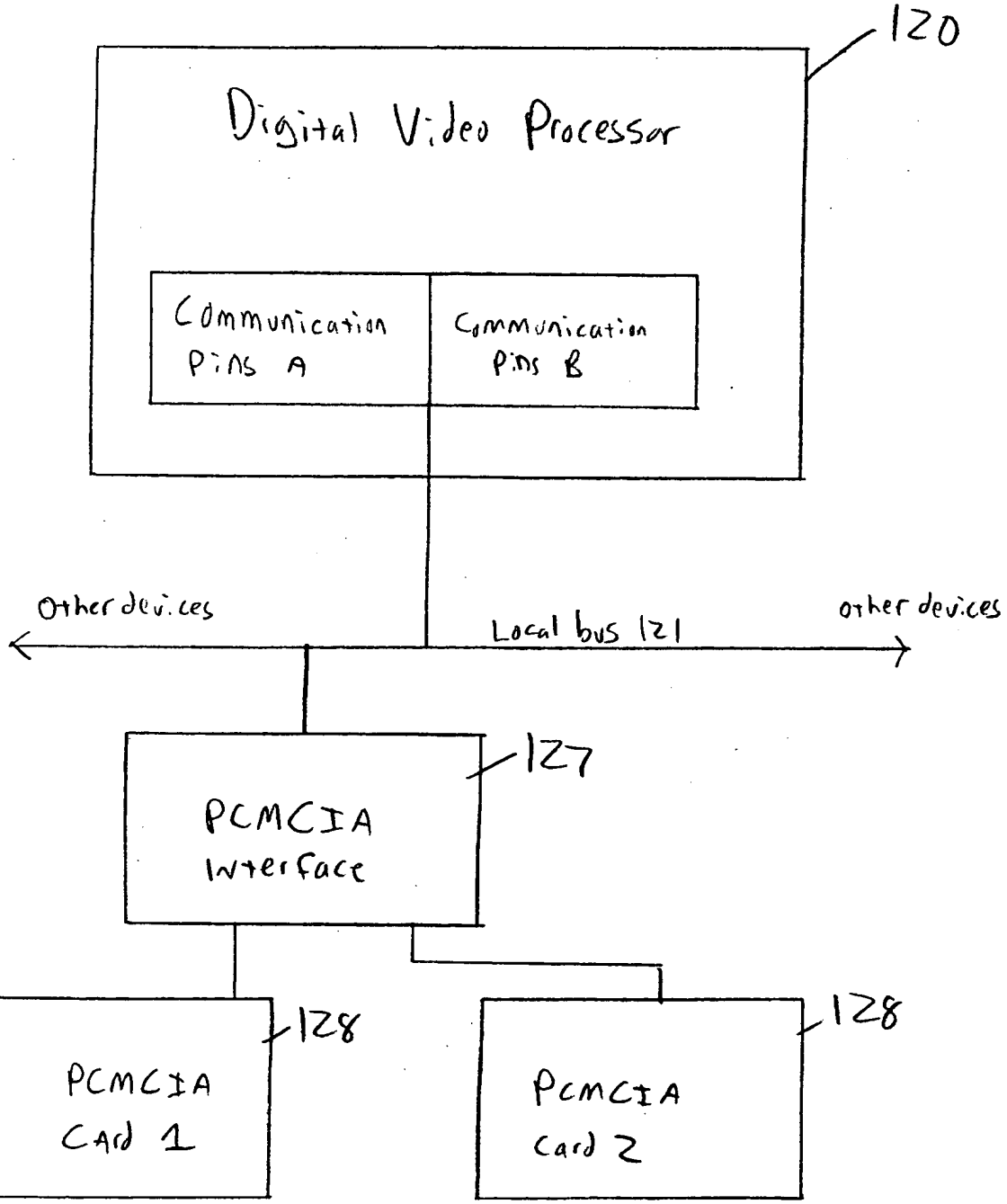
120
Digital Video Processor
Communication Pins A
Communication Pins B
Other devices
Local bus 121
other devices
127
PCMCIA Interface
128
PCMCIA Card 1
128
PCMCIA Card 2

Fig 2

PCMCIA Signals			Digital video processor signals			
Pin #	Mem Map	I/O + Mem	A Pin #	A Signal	B Pin #	B Signal
1	GND	GND	-	GND	-	GND
2	D3	D3	254	ARM_D3	254	ARM_D3
3	D4	D4	253	ARM_D4	253	ARM_D4
4	D5	D5	252	ARM_D5	252	ARM_D5
5	D6	D6	251	ARM_D6	251	ARM_D6
6	D7	D7	248	ARM_D7	248	ARM_D7
7	CE1#	CE1#	204	CFE1	204	CFE1
8	A10	A10	274	ARM_A10	274	ARM_A10
9	OE#	OE#	203	CFOE	203	CFOE
10	A11	A11	-	GND	-	GND
11	A9	A9	275	ARM_A9	275	ARM_A9
12	A8	A8	276	ARM_A8	276	ARM_A8
13	A13	A13	-	GND	-	GND
14	A14	A14	-	GND	-	GND
15	WE#	WE#	221	EM_WE	221	EM_WE
16	READY	IREQ#	47	GIO6	38	GIO14
17	VCC	VCC	-	VCC	-	VCC
18	VPP	VPP	-	VPP	-	VPP
19	A16	A16	-	GND	-	GND
20	A15	A15	-	GND	-	GND
21	A12	A12	-	GND	-	GND
22	A7	A7	277	ARM_A7	277	ARM_A7
23	A6	A6	278	ARM_A6	278	ARM_A6
24	A5	A5	281	ARM_A5	281	ARM_A5
25	A4	A4	282	ARM_A4	282	ARM_A4
26	A3	A3	283	ARM_A3	283	ARM_A3
27	A2	A2	284	ARM_A2	284	ARM_A2
28	A1	A1	285	ARM_A1	285	ARM_A1
29	A0	A0	286	ARM_A0	286	ARM_A0
30	D0	D0	257	ARM_D0	257	ARM_D0
31	D1	D1	256	ARM_D1	256	ARM_D1
32	D2	D2	255	ARM_D2	255	ARM_D2
33	WP	IOIS16#	30, 208	GIO21, IOIS16	20, 208	GIO29, IOIS16
34	GND	GND	-	GND	-	GND

Fig 3A

PCMCIA Signals			Digital Video processor signals			
Pin #	Mem Map	I/O + Mem	A Pin #	A Signal	B Pin #	B Signal
35	GND	GND	-	GND	-	GND
36	CD1#	CD1#	53	GIO0	45	GIO8
37	D11	D11	244	ARM_D11	244	ARM_D11
38	D12	D12	243	ARM_D12	243	ARM_D12
39	D13	D13	242	ARM_D13	242	ARM_D13
40	D14	D14	241	ARM_D14	241	ARM_D14
41	D15	D15	240	ARM_D15	240	ARM_D15
42	CE2#	CE2#	205	CFE2	205	CFE2
43	VS1#	VS1#	35	GIO16	27	GIO24
44	-	IORD#	209	CFIORD	209	CFIORD
45	-	IOWR#	210	CFIOWR	210	CFIOWR
46	A17	A17	-	GND	-	GND
47	A18	A18	-	GND	-	GND
48	A19	A19	-	GND	-	GND
49	A20	A20	-	GND	-	GND
50	A21	A21	-	GND	-	GND
51	VCC	VCC	-	VCC	-	VCC
52	VPP	VPP	-	VPP	-	VPP
53	A22	A22	-	GND	-	GND
54	A23	A23	-	GND	-	GND
55	A24	A24	-	GND	-	GND
56	A25	A25	-	GND	-	GND
57	VS2#	VS2#	34	GIO17	26	GIO25
58	RESET	RESET	31	GIO20	23	GIO28
59	WAIT#	WAIT#	206	CFWAIT	206	CFWAIT
60	-	INPACK#	-	-	-	-
61	REG#	REG#	260	ARM_A22	260	ARM_A22
62	BVD2	SPKR#	50	GIO3	42	GIO11
63	BVD1	STSCHG#	51	GIO2	43	GIO10
64	D8	D8	247	ARM_D8	247	ARM_D8
65	D9	D9	246	ARM_D9	246	ARM_D9
66	D10	D10	245	ARM_D10	245	ARM_D10
67	CD2#	CD2#	52	GIO0	44	GIO8
68	GND	GND	-	GND	-	GND

Fig 3B

Digital vid. proc 120		System	
Pin #	**Signal**	**Signal**	**Use**
53	GIO0		*Never use*
52	GIO1	A_PWR	slot A power supply enable
51	GIO2	A_BVD1	slot A BVD1/ STSCHG#
50	GIO3	A_CD	slot A card detect
49	GIO4	O_BSFX00	Audio interrupt
48	GIO5	O_RS0	Audio reset
47	GIO6	A_RDY	slot A READY/IREQ#
46	GIO7	TV_CIR	CIR
45	GIO8	B_CD	slot B card detect
44	GIO9	B_PWR	slot B power supply enable
43	GIO10	B_BVD1	slot B BVD1/ STSCHG#
42	GIO11	B_BVD2	slot B BVD2/ SPKR#
41	GIO12	M_IRQ	Media Processor interrupt
40	GIO13	O_HINT0	Audio interrupt
38	GIO14	B_RDY	slot B READY/IREQ#
36	GIO15	TV_CL	TV audio clock interrupt
35	GIO16	A_VS1	slot A VS1#
34	GIO17	A_VS2	slot A VS2#
33	GIO18	A_33_EN	slot A voltage select: '0' for 5.0v, '1' for 3.3v
32	GIO19	A_OE	slot A output enable: '0' enables slot, '1' disables slot
31	GIO20	A_RESET	slot A RESET
30	GIO21	A_WP	slot A WP
29	GIO22	F_VPP	FLASH program enable
28	GIO23	M_RSN	Media processor reset
27	GIO24	B_VS1	slot B VS1#
26	GIO25	B_VS2	slot B VS2#
25	GIO26	B_33_EN	slot B voltage select: '0' for 5.0v, '1' for 3.3v
24	GIO27	B_OE	slot B output enable: '0' enables slot, '1' disables slot
23	GIO28	B_RESET	slot B RESET
20	GIO29	B_WP	slot B WP
19	GIO30		
18	GIO31		test signal
17	GIO32		test signal
16	GIO33		test signal

Fig. 4

Media proc. 100		System	
Pin #	**Signal**	**Signal**	**Use**
53	GIO0		*Never use*
52	GIO1	TV_CL	TV audio clock interrupt
51	GIO2		
50	GIO3	M_HINT0	MP audio DSP interrupt
49	GIO4	M_BSFX01	MP DA150 interrupt
48	GIO5	M_RS1	MP audio DSP reset
47	GIO6		
46	GIO7	M_IRQ	Media Processor interrupt
45	GIO8		
44	GIO9	TV_CL	TV audio clock interrupt
43	GIO10		
42	GIO11		
41	GIO12		
40	GIO13		
38	GIO14		
36	GIO15		
35	GIO16		
34	GIO17		
33	GIO18		
32	GIO19		
31	GIO20		
30	GIO21		
29	GIO22		
28	GIO23		
27	GIO24		
26	GIO25		
25	GIO26		
24	GIO27		
23	GIO28		
20	GIO29		
19	GIO30		
18	GIO31		test signal
17	GIO32		test signal
16	GIO33		test signal

Fig. 5

Memory Map

Area Name	Start Address	End Address	Size (bytes)
Socket A Attribute Space	0x0520:0000	0x0520:ffff	64K
Socket B Attribute Space	0x0528:0000	0x0528:ffff	64K
Socket A Memory Space	0x0530:0000	0x0530:ffff	64K
Socket B Memory Space	0x0538:0000	0x0538:ffff	64K
Socket A I/O Space	0x0560:0000	0x0560:ffff	64K
Socket B I/O Space	0x0568:0000	0x0568:ffff	64K

Fig. 6

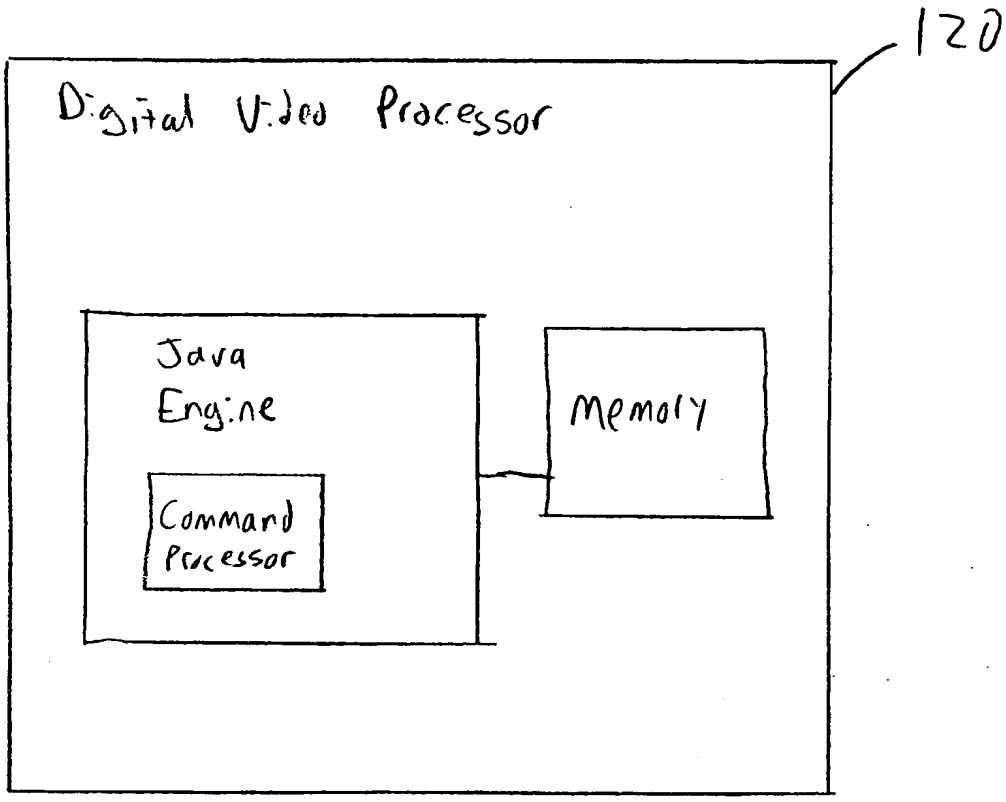
120
Digital Video Processor
Java
Engine
Command
Processor
Memory

Fig. 7